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EXAMINER	
CULBERT, ROBERTS P	
ART UNIT	**PAPER NUMBER**
1763	

DATE MAILED: 06/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/766,087	ADAMS ET AL.	
	Examiner	Art Unit	
	Roberts Culbert	1763	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *47-83 and 116-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *47-83 and 116-119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 47-51, 56-58, 60, 61, 75 and 77-79 are rejected under 35 U.S.C. 102(a) as being anticipated by International Application Publication WO9936948 A1 to Adams et al.

Regarding Claim 47, Adams et al. teach a method for fabricating a microelectromechanical (MEMS) apparatus comprising: forming first trenches on a first side of a substrate (Page 15, Lines 18-22), forming a layer of dielectric material on the first side of the substrate, and filling the first trenches with the dielectric material to provide electrical isolation (Page 16, Lines 11-19), patterning a masking layer on a second side of the substrate that is opposite to the first side of the substrate (Page 17, Lines 1-10), forming vias on the first side of the substrate (reads on at least Page 15, Lines 18-22 or Page 18, Lines 13-19), metallizing the first side of the substrate (Page 19, Lines 13-19) forming second trenches on the first side of the substrate to define structures (Page 18, Lines 10-16), deeply etching the second side of the substrate to form blades (Page 17, Line 20 – Page 18 Line 1), and etching to release the structures (Page 18, Lines 3-12).

Regarding Claim 48, Adams et al. teach attaching a protective structure to the second side of the substrate prior to etching. (Page 17, Lines 1-10)

Regarding Claim 49, Adams et al. teach that the substrate is a silicon wafer. (Page 12, Lines 1-5)

Regarding Claim 50, Adams et al. teach attaching a protective lid to the first side. (Page 15, Lines 5-9)

Regarding Claim 51, Adams et al. teach that the dielectric is silicon dioxide (Page 16, Lines 11-13)

Regarding Claim 56, Adams et al. teach a method for fabricating a microelectromechanical apparatus, comprising: patterning a masking layer on a second side of a substrate having a second side that is opposite to a first side of the substrate (Page 17, Lines 1-10), deeply etching the second side of the substrate to form blades (Page 17, Line 20 – Page 18 Line 1), attaching a protective structure to the second side of the substrate (Page 17, Lines 1-10), forming first trenches on the first side of the substrate (Page 15, Lines 18-22), forming a layer of dielectric material on the first side of the substrate and filling the first trenches with the dielectric material to provide electrical isolation (Page 16, Lines 11-19), forming vias on the first side of the substrate (reads on at least Page 15, Lines 18-22 or Page 18, Lines 13-19), metallizing the first side of the substrate, forming second trenches on the first side of the substrate to define structures (Page 18, Lines 10-16), etching to release the structures (Page 18, Lines 3-12).

Regarding Claim 57 Adams et al. teach that the substrate is a silicon wafer. (Page 12, Lines 1-5)

Regarding Claim 58, Adams et al. teach attaching a protective lid to the first side. (Page 15, Lines 5-9)

Regarding Claim 60, Adams et al. teach that the protective structure has a recess facing the second side of the substrate (See Figure 5)

Regarding Claim 61, Adams et al. teach that the dielectric is silicon dioxide (Page 16, Lines 11-13)

Regarding Claim 75, Adams et al. teach patterning a masking layer on a second side of the substrate that is opposite to a first side of the substrate (Page 17, Lines 1-10), attaching spacer substrate (photoresist) to the second side of the substrate (Page 17, Lines 3-10) forming first trenches on the first side of the substrate (Page 15, Lines 18-22), forming a layer of dielectric material on the first side of the substrate and filling the first trenches with the dielectric material to provide electrical isolation (Page 16,

Lines 11-19), forming vias on the first side of the substrate (reads on at least Page 15, Lines 18-22 or Page 18, Lines 13-19), metallizing the first side of the substrate (Page 19, Lines 13-19), forming second trenches (Page 18, Lines 10-16) on the first side of the substrate to define structures, etching an opening through the spacer substrate to expose the masking layer on the second side of the substrate (Page 17, Lines 1-12), deeply etching the second side of the substrate to form blades (Page 17, Line 20 – Page 18 Line 1), and etching to release the structures (Page 18, Lines 3-12).

Regarding Claim 77, Adams et al. teach that the substrate is a silicon wafer. (Page 12, Lines 1-5)

Regarding Claim 78, Adams et al. teach attaching a protective lid to the first side. (Page 15, Lines 5-9)

Regarding Claim 79, Adams et al. teach that the dielectric is silicon dioxide (Page 16, Lines 11-13)

Claims 47-51, 56-58, 60, 61, 75 and 77-79 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent 6,074,890 to Yao et al.

Regarding Claim 47, Yao et al. teaches a method for fabricating a microelectromechanical (MEMS) apparatus comprising: forming trenches on a first side of a substrate (Figure 4a), forming a layer of dielectric material on the first side of a substrate and filling trenches with the dielectric material (Figures 4b and 4c), patterning a masking layer (fourth mask) on a second side of the SOI substrate that is opposite to the first side of the substrate (Col. 5, Lines 55-58), forming vias on the first side of the SOI substrate that extend through a buried oxide layer (figure 4c), metallizing the first side of the SOI substrate (Col. 5, Lines 64-67), forming trenches on the first side of the substrate to define structures (Figure 5a), deeply etching the second side of the SOI substrate to form blades, and etching to release the structures (Col. 5, Lines 55-60).

Regarding Claims 48 and 56, Yao et al. further teaches the additional step of attaching a protective structure (oxide mask) to the second side of the substrate. (Col. 5, Lines 34-35)

Regarding Claim 75, Yao et al. teaches the additional steps of attaching a spacer member (fourth mask) to the second side of the substrate and etching an opening (patterning) to expose the masking layer (oxide layer)

Regarding Claims 51, 61, and 79, Yao et al. teach that the dielectric is silicon dioxide. (Col. 5, Lines 38-42)

Regarding Claims 49, 57 and 77, Yao et al. teach that the substrate is a silicon wafer. (Col. 5, Lines 13-17)

Regarding Claims 50, 58 and 78, Yao et al. teaches attaching a protective lid (first mask) to the first side. (Col. 5, Lines 23-38)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 52, 53, 62, 63, 80 and 81 are rejected under 35 U.S.C. 103(a) as being unpatentable over International Application Publication WO9936948 A1 to Adams et al. in view of U.S. Patent 5,719,073 to Shaw et al.

As applied above, Adams et al. teach the method of the invention substantially as claimed, but do not teach depositing a second metal layer or forming a passivation layer on the first side of the substrate after metallizing.

Shaw et al. teach a method of forming an accelerometer comprising: forming metalized trenches in a silicon substrate, forming a second metal layer (Col. 18, Line 33- Col 20, Line 6) and forming a passivation layer on the first side of the substrate after metallizing (Col. 6, Lines 59-62).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional metal layer or passivaton layers as recited in Shaw et al. in order to suitably process the MEMS substrate to form an suspended MEMS structure such as an accelerometer in the well-known manner.

Claims 54, 55, 64, 65, 82 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over International Application Publication WO9936948 A1 to Adams et al. in view of U.S. Patent 5,591,679 to Jakobsen et al.

As applied above, Adams et al. teach the method of the invention substantially as claimed, but do not teach bonding a protective layer of glass to the second side of the MEMS device substrate.

Jakobsen et al. teach that it is conventional in the art of MEMS processing to seal sensor devices by attaching a glass or silicon wafer lid to form a sealed MEMS device such as a pressure sensor. (Col. 7, Lines 20-27)

It would have been obvious to one of ordinary skill in the art at the time of invention to use a glass or silicon wafer lid to seal the MEMS device and provide suitable protection for the device.

Claims 52, 53, 62, 63, 66-72, 80, 81 and 119 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,719,073 to Shaw et al.

Regarding Claim 66, Yao et al. teaches a method for fabricating a microelectromechanical (MEMS) apparatus comprising: forming a layer of dielectric material on the first side of a SOI (silicon-on-insulator) substrate (Col. 5, Lines 34-35), patterning a masking layer on a second side of the SOI

substrate that is opposite to the first side of the SOI substrate (Col. 5, Lines 55-58), forming vias on the first side of the SOI substrate that extend through a buried oxide layer (Figure 4c), metallizing the first side of the SOI substrate (Col. 5, Lines 64-67), forming trenches on the first side of the SOI substrate to define structures (Figure 4a), deeply etching the second side of the SOI substrate to form blades, and etching to release the structures (Col. 5, Lines 55-60).

Yao et al. do not teach forming a passivation layer on the first side of the substrate after metallizing.

Shaw et al. teach a method of forming an accelerometer comprising: forming metalized trenches in a silicon substrate, and forming a passivation layer on the first side of the substrate after metallizing (Col. 6, Lines 59-62).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional passivaton layer as recited in Shaw et al. in order to prevent shorting between moving structures as recited in Shaw et al.

Regarding Claim 67, Yao et al. teaches attaching a protective structure (fourth mask) to the second side of the SOI substrate prior to etching to release the structures. (Col. 5, Lines 32-33)

Regarding Claim 68, Yao et al. teaches using a SOI wafer. (Col. 3, Lines 15-20)

Regarding Claim 69, Shaw et al. teaches attaching a protective lid to the first side of the SOI substrate. (Col. 6, Lines 59-62)

Regarding Claim 70, Yao et al. teaches the dielectric material is silicon dioxide. (Col. 5, Lines 33-36)

Regarding Claim 71, Yao et al. does not teach depositing a second metal layer after metallizing. Shaw et al. teaches depositing a second metal layer on the after metallizing (Col. 18, Line 33- Col 20, Line 6).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional metal layer as recited in Shaw et al. in order to suitably process the MEMS substrate to form a completed MEMS structure in the well-known manner.

Regarding Claim 72, Yao et al. teaches etching to the buried oxide layer. (Figure 4d)

Regarding Claims 52, 62, and 80, as applied above to claims 47-51, 56- 61, 75 and 77-79, Yao et al teach the method of the invention substantially as claimed, but do not teach forming a second metal layer on the first side of the substrate after metallizing.

Shaw et al. teach a method of forming an accelerometer comprising: forming metalized trenches in a silicon substrate, and forming a second metal layer on the first side of the substrate after metallizing (Col. 18, Line 33- Col 20, Line 6).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional metal layer as recited in Shaw et al. in order to increase the mass of the suspended-beam MEMS device as recited in Shaw et al.

Regarding Claims 53, 63 and 81, as applied above to claims 47-51, 56- 61, 75 and 77-79, Yao et al teach the method of the invention substantially as claimed, but do not teach forming a passivation layer on the first side of the substrate after metallizing.

Shaw et al. teach a method of forming an accelerometer comprising: forming metalized trenches in a silicon substrate, and forming a passivation layer on the first side of the substrate after metallizing (Col. 6, Lines 59-62).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional passivation layer as recited in Shaw et al. in order to prevent shorting between moving structures as recited in Shaw et al.

Regarding Claim 119, Yao et al. teaches a method for fabricating a microelectromechanical (MEMS) apparatus comprising: forming a layer of dielectric material on the first side of a SOI (silicon-on-insulator) substrate (Col. 5, Lines 34-35), patterning a masking layer on a second side of the SOI substrate that is opposite to the first side of the SOI substrate and filling the trenches with the dielectric (Col. 5, Lines 55-58 and Figures 4a-4c), forming vias on the first side of the SOI substrate that extend through a buried oxide layer (Figure 4c), metallizing the first side of the SOI substrate (Col. 5, Lines 64-67), forming trenches on the first side of the SOI substrate to define structures (Figure 4a), deeply etching

the second side of the SOI substrate to form blades, and etching to release the structures (Col. 5, Lines 55-60). Yao et al. teaches attaching a protective lid (first mask) to the first side. (Col. 5, Lines 23-38)

Yao et al. do not teach forming a second metal layer on the first side of the substrate after metallizing.

Shaw et al. teach a method of forming an accelerometer comprising: forming metalized trenches in a silicon substrate, and forming a second metal layer on the first side of the substrate after metallizing (Col. 18, Line 33- Col 20, Line 6).

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to use the additional metal layer as recited in Shaw et al. in order to increase the mass of the suspended-beam MEMS device as recited in Shaw et al.

Claims 55, 65 and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,591,679 to Jakobsen et al.

As applied above, Yao et al. teach the method of the invention substantially as claimed, but do not teach bonding a protective layer of glass or silicon to the second side of the MEMS device substrate.

Jakobsen et al. teach that it is conventional in the art of MEMS processing to seal sensor devices by attaching a glass or silicon wafer lid to form a sealed MEMS device such as a pressure sensor. (Col. 7, Lines 20-27)

It would have been obvious to one of ordinary skill in the art at the time of invention to use a glass or silicon wafer lid to seal the MEMS device and provide suitable protection for the device.

Claims 59 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 6,030,887 to Desai et al.

As applied above to claims 47-51, 56- 61, 75 and 77-79, Yao et al teach the method of the invention substantially as claimed, but do not teach thinning the substrate prior to forming trenches.

However, it is known in the art of MEMS fabrication to thin a wafer prior to forming devices in order to provide a wafer having suitable thickness for the device. For example, Desai et al. teaches thinning a substrate wafer in order to provide suitable thickness to a MEMS device. (Col. 7, Lines 63-66)

It would have been obvious to one of ordinary skill in the art at the time of invention to use a suitably thinned wafer substrate in order to provide a stock material having thickness suited to MEMS fabrication.

Claims 74 and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,719,073 to Shaw et al. and in further view of U.S. Patent 5,591,679 to Jakobsen et al.

As applied above, Yao et al. in view of Shaw teach the method of the invention substantially as claimed, but do not teach bonding a protective layer of glass or silicon to the second side of the MEMS device substrate.

Jakobsen et al. teach that it is conventional in the art of MEMS processing to seal sensor devices by attaching a glass or silicon wafer lid to form a sealed MEMS device such as a pressure sensor. (Col. 7, Lines 20-27)

It would have been obvious to one of ordinary skill in the art at the time of invention to use a glass or silicon wafer lid to seal the MEMS device and provide suitable protection for the device.

Claims 54, 64, and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,719,073 to Shaw et al and in view of U.S. Patent 6,428,713 to Christenson et al.

As applied above to claims 47-51, 56-58, 60, 61, 75 and 77-79, Yao et al. teaches the method of the invention substantially as claimed, but do not teach bonding a base wafer to the second surface before etching to release the structures.

Christenson et al. teach bonding a base wafer to a second surface before etching to release MEMS structures. (Col. 8, Line 62- Col. 10, Line 59)

It would have been obvious to one of ordinary skill in the art at the time of invention to bond a base wafer to the substrate of Yao et al. in order to provide support for the substrate during front-side processing and to take advantage of the etching technique of Christenson that prevents sticking between projections of the MEMS device. (Col. 12, Lines 37-48)

Claims 73, and 116 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,719,073 to Shaw et al and in view of U.S. Patent 6,428,713 to Christenson et al.

As applied above to claims 47-51, 56-58, 60, 61, 75 and 77-79, Yao et al. in view of Shaw et al. teaches the method of the invention substantially as claimed, but do not teach bonding a base wafer to the second surface before etching to release the structures.

Christenson et al. teach bonding a base wafer to a second surface before etching to release MEMS structures. (Col. 8, Line 62- Col. 10, Line 59)

It would have been obvious to one of ordinary skill in the art at the time of invention to bond a base wafer to the substrate of Yao et al. in order to provide support for the substrate during front-side processing and to take advantage of the etching technique of Christenson that prevents sticking between projections of the MEMS device. (Col. 12, Lines 37-48)

Claim 117 is rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 6,074,890 to Yao et al. in view of U.S. Patent 5,719,073 to Shaw et al and U.S. Patent 6,030,887 to Desai et al. and in further view of U.S. Patent 6,428,713 to Christenson et al.

As applied above to claims 47-51, 56-58, 60, 61, 75 and 77-79, Yao et al. in view of Shaw et al. teaches the method of the invention substantially as claimed, but do not teach thinning the substrate or bonding a base wafer to the second surface before etching to release the structures.

However, it is known in the art of MEMS fabrication to thin a wafer prior to forming devices in order to provide a wafer having suitable thickness for the device. For example, Desai et al. teaches thinning a substrate wafer in order to provide suitable thickness to a MEMS device. (Col. 7, Lines 63-66)

It would have been obvious to one of ordinary skill in the art at the time of invention to use a suitably thinned wafer substrate in order to provide a stock material having thickness suited to MEMS fabrication.

Christenson et al. teach bonding a base wafer to a second surface before etching to release MEMS structures. (Col. 8, Line 62- Col. 10, Line 59)

It would have been obvious to one of ordinary skill in the art at the time of invention to bond a base wafer to the substrate of Yao et al. in order to provide support for the substrate during front-side processing and to take advantage of the etching technique of Christenson that prevents sticking between projections of the MEMS device. (Col. 12, Lines 37-48)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Roberts Culbert whose telephone number is (571) 272-1433. The examiner can normally be reached on Monday-Friday (8:30-5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Parviz Hassanzadeh can be reached on (571) 272-1435. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

R. Culbert

PARVIZ HASSENZADEH
SUPERVISORY PATENT EXAMINER